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EXAMINER	
WEST, JEFFREY R	
ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,195	YASALA, RAJU	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 25, 26, 29 and 30 are objected to because of the following informalities:

In claim 25, line 7, to avoid problems of antecedent basis in claim 28, "adapted to measure" should be ---adapted to sense---.

In claim 25, line 10, "of target" should be ---of the target---.

In claim 26, line 2, to avoid problems of antecedent basis, "calculated percentage" should be ---determined percentage---.

In claim 29, line 4, "executing software" should be --- executing a software---.

In claim 30, line 2, to avoid problems of antecedent basis, "the current" should be ---the amount of current---.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 25-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 25 recites, "the target memory comprising a maximum current utility adapted to cause the target processor to consume increased amounts of current by the target processor at peak current usage times to increase processing speeds at peak current usage times."

The specification describes this limitation at best on pages 3-4, specifically:

"Target system performance bottlenecks may be discovered and software architects will find processor utilization data useful during application turning to verify performance effects among various software application versions, as shown in Figure 2. Data associated with program A.1 (version 1 of program A) 200 displays significant processor utilization values at time units 4, 6, and 9. After the software architect modifies program A.1 (thereby creating version A.2) to utilize more processor resources at those times, the system 100 may be used to compare program A.1 200 with the optimized program A.2 210. The system 100 plots data for both programs A.1 200 and A.2 210 to allow the system architect to verify whether or not program A.2 210 is an improvement over the previous version." (pages 3-4, paragraph 0014).

This section of the specification, in addition to Figure 2, describes that the amount of current consumed is controlled by creating a new version of the "% Processor Utilization Program". On page 2, paragraph 0010, the specification explicitly states that the "software application known as the utilization application controls the system 100 during data acquisition of the target system's processor 115" and the "utilization application is stored in the system memory 130 and executed by the system processor 135". Since the specification indicates that the increase of current consumption is controlled by the processor utilization program/application and also indicates that this processor utilization program/application is stored and executed by the host system and not the target system, the specification does not adequately enable one having ordinary skill in the

art to make/use the claimed invention of "the target memory comprising a maximum current utility adapted to cause the target processor to consume increased amounts of current by the target processor at peak current usage times to increase processing speeds at peak current usage times."

Claim 29 recites, "continuously repeating the sensing, transmitting and comparing steps for a duration of said execution of said software application; calculating, at a host processor, a percentage of the maximum current value being consumed by the target processor over time and identifying peak use times for said execution of said software application" wherein the comparing step comprises "comparing said amount of current against a maximum current value for the target processor but stored in a host memory".

This section of claim 29 is not sufficiently enabled by the specification because these is no disclosure in the instant specification of "continuously repeating the sensing, transmitting and comparing steps for a duration of said execution of said software application". Pages 4-5 of the specification recite:

"The target application is started for a pre-determined amount of time at block 330 and the effects of that application on the target processor 115 are collected by the current sensor 145 and logged at block 340. After the target software application has stopped executing, the MCU is started at block 350 and the effects of the MCU on the target processor 115 are collected by the current sensor 145 and logged at block 360. Upon completion of data collection at block 360, an average maximum processor current value is calculated at block 370. The host system 100 now has enough data at block 380 to calculate the percentage of processor usage caused by executing the target application(s). The percent of processor utilization is obtained by dividing the current consumed by the target processor 115 during execution of the software application(s) by the average maximum processor current consumed

when the MCU was executed. The host system 100 plots the percent processor usage versus time at block 390" (pages 4-5, paragraph 0015).

As can be seen by the above disclosure, the "effects of the MCU on the target processor 114 are collected by the current sensor 145 and logged at block 360" after which "an average maximum processor current value is calculated at block 370". As claimed, this "average maximum processor current value" is used in the comparison step. The disclosure, however, explicitly states that blocks 360 and 370 are performed "After the target software application has stopped executing". Additionally, there is no disclosure of repeating the sensing, transmitting, and comparing during execution of the target software application. Therefore, the specification does not sufficiently enable one having ordinary skill in the art to perform "continuously repeating the sensing, transmitting and comparing steps for a duration of said execution of said software application" and does not sufficiently enable one having ordinary skill in the art to make/use the invention as claimed.

Claims 26-28, 30, and 31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement because they incorporate the lack of enablement present in their respective parent claims.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 25-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 25 is considered to be vague and indefinite because line 4 attempts to further limit "the target processor part" to also comprise a "target memory". There is, however, no previous mention of any "target processor part" only a "target processor" and since a "target processor" cannot comprise a "target memory", it is unclear to one having ordinary skill in the art as to what "the target processor part" refers.

Claim 25 is also rejected under 35 U.S.C. 112, second paragraph, because it contains the confusing limitation of "cause the target processor to consume increased amount of current by the target processor", bridging lines 12 to 13.

Claim 25 is further rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 25 presents "a power supply...the target processor part...a host...a sensor...the host memory...the target memory..." The target memory, however, is defined as "comprising a maximum current utility adapted to cause the target processor to consume increased amounts of current by the target processor at peak current usage times to increase the processing speeds at peak current usage times." This limitation for the "target memory" contains no structural relationship to the other system components (i.e. the power supply, the target processor part, the host, the sensor, or the host memory) and does not use any of the data obtained by the other system components, thereby arriving in a gap between the necessary structural connections.

Claim 29 is considered to be vague and indefinite because it contains the confusing limitation of "comparing said amount of current against a maximum current value for the target processor but stored in a host memory". In this limitation, it is unclear to one having ordinary skill in the art as to what "but stored in a host memory" is to further limit.

Claim 29 is also rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. Claim 29 presents a method comprising the steps of "sensing..., transmitting..., comparing...continuously repeating...calculating...and increasing..." The steps of continuously repeating and calculating, however, are defined as "continuously repeating the sensing, transmitting and comparing steps for a duration of said execution of said software application; calculating, at a host processor, a percentage of the maximum current value being consumed by the target processor over time and identifying peak use times for said execution of said software application". These two steps contain no apparent relationship thereby arriving at a gap between the steps, specifically because the continuous repeating of the sensing, transmitting, and comparing steps does not arrive at any result that is used in the subsequent step of calculating (i.e. a step is missing where the result of the comparing is used in the further steps of the method).

Claim 30 is considered to be vague and indefinite because it recites, in lines 2-3, "comparing of the current being consumed by the target processor against a maximum current value". Parent claim 29, however, already presents a limitation for

"a maximum current value" in line 6 and refers to "the maximum current value" in line 10. It is therefore unclear to one having ordinary skill in the art whether the limitation for "a maximum current value" in claim 30 is the same as the "maximum current value" of parent claim 29, or if this recitation in claim 30 refers to a different maximum current value.

Claims 26-28 and 31 are rejected under 35 U.S.C. 112, second paragraph, because they incorporate the lack of clarity present in their respective parent claims

Response to Arguments

6. Applicant's arguments with respect to claims 25-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

U.S. Patent No. 6,304,978 to Horigan et al. discloses a system, for a processor having a power line, to determine processor utilization, the system comprising a sensor ("255") coupled to the power line ("247") for measuring a current magnitude in the power line as the current being consumed by the processor (column 5, lines 45-47 and Figure 2).

U.S. Patent No. 6,721,672 to Spitaels et al. discloses a system, for a processor having a power line, to determine processor utilization (column 6, lines 18-21), the

system comprising a sensor coupled to the power line for measuring a current magnitude of the power line indicating current being consumed by the processor (column 6, lines 35-39). Spitaels discloses that the measured current is compared to a maximum current value indicative of current consumed by the processor when fully utilized to insure that the maximum current is utilized (column 8, lines 48-55 and column 9, lines 43-52) using a software application means (column 5, lines 61-64). Spitaels discloses using a software application (column 8, lines 35-38) to determine a maximum current value indicative of current consumed by the processor when fully utilized (column 8, lines 50-58). Spitaels discloses using a software application to cause the processor to be fully utilized (column 6, lines 3-4 and 10-21).

U.S. Patent No. 6,057,839 to Advani et al. teaches a visualization tool for graphically displaying trace data produced by a parallel processing computer comprising a host including a host processor and host memory storing a utilization utility adapted to be stored in the host memory and executed by the host processor (column 4, lines 46-64), the utilization utility further adapted to calculate utilization information of a target processor (column 5, lines 51-57) as well as generate a graphical representation of the processor utilization (column 5, lines 58-60) to optimize a software application executing on the target processor in response to the calculated target processor utilization information (column 2, lines 15-20).

U.S. Patent No. 4,823,075 to Alley teaches a current sensor using a Hall-effect device with feedback including a Hall-effect sensor for sensing the current (column 2, lines 16-39).

U.S. Patent No. 6,636,976 to Grochowski et al. teaches a mechanism to control di/dt for a microprocessor.

U.S. Patent No. 6,457,131 to Kuemerle teaches a system and method for power optimization in parallel units.

U.S. Patent No. 6,105,142 to Goff et al. teaches an intelligent power management interface for computer system hardware.

U.S. Patent No. 5,692,204 to Rawson et al. teaches a method and apparatus for computer system power management.

U.S. Patent No. 6,574,739 to Kung et al. teaches dynamic power saving by monitoring CPU utilization.

U.S. Patent Application Publication No. 2002/0194509 to Plante et al. teaches a method and system for using idle threads to adaptive throttle a computer.

U.S. Patent Application Publication No. 2002/0181311 to Miyauchi teaches a semiconductor memory unit in which power consumption can be restricted.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jrw
September 6, 2005

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